Milan Shah

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Education

Purdue University, West Lafayette, IN **Aug 2025 – Present**
B.S. Computer Engineering – Expected Graduation: May 2028
GPA: 4.0/4.0 — Dean's List and Semester Honors for all completed semesters

Experience

The Hill Mortgage Company, Aurora, IL — *Software Development Engineer* **Jun 2026 – Present**
- Architected a **JWT**-authenticated **REST API** (**CodeIgniter/PHP**, **MySQL**) for a loan-origination platform scaling to **100,000+ annual loans**, with an ENUM-driven **state machine**, regulatory co-borrower income/asset separation, and tokenized links that cut onboarding time by **40%**
- Built an **event-driven processing engine** fanning credit, flood, and title verification into non-blocking **async worker pools** with **idempotency** safeguards, plus an **automated underwriting service** parsing **GSE XML** (Fannie DU / Freddie LPA) through a **JSON-defined rules engine** — auto-approving **70% of clean files** and cutting processing time by **55%**

Schema, Naperville, IL — *Founder* **Nov 2025 – Present**
- Built a desktop **EDA suite** in **C/C++** and **Qt6** — a **KiCad**/**Altium**-class tool spanning schematic capture, PCB layout, and DRC validation — exposing a structured command interface that maps natural-language agent output to document operations, cutting schematic-to-routed-board time by **60%**
- Engineered a **four-stage multi-agent pipeline** (**Gemini API**) — conversational planning, RAG-based component selection via an **hnswlib vector DB** with live SnapEDA integration, spatial layout, and command synthesis — turning a single natural-language prompt into a routed PCB design at an **85% DRC-pass rate**
- **Fine-tuned a custom Qwen LLM** on RunPod (containerized **Docker**/**Linux** GPU) to improve geometric reasoning for hardware layout, boosting precision in component placement, trace routing, and clearance satisfaction by **30%**

TRACE Lab & Humanoid Robotics Club, West Lafayette, IN — *Researcher* **Aug 2025 – May 2026**
- **Published** in **Journal of Purdue Undergraduate Research** (JPUR) on **reinforcement-learning** control for humanoid robotics, training neural policies in **PyTorch** within **NVIDIA Isaac Sim** and deploying to a Jetson Nano over **ROS2**
- **Achieved 91% simulation** and **83% real-world** return accuracy by implementing and tuning **PPO algorithms** on the SmolVLA **computer-vision** dataset in **Python**, with research expanding to other racket sports

Purdue University, West Lafayette, IN — *Undergraduate TA — Circuit Analysis I* **Jan 2025 – May 2026**
- **Instructed 100+ students** in office hours on core EE concepts — Thevenin/Norton equivalents, AC steady-state analysis, magnetically coupled circuits, and MOSFETs — reinforced through **MATLAB** circuit simulation
- **Led weekly recitations of 50 students**, delivering supplementary lecture material and working through problem sets

Argonne National Lab & Northwestern University, Lemont/Chicago, IL — *Researcher* **Sep 2024 – Aug 2025**
- Collaborated with NUPOC on **prosthetic development** research in synchrotron science at the ANL Advanced Photon Source beamline, **presenting to 300+ attendees** at a research symposium
- Developed **simulation-modeling** pipelines in **Python** (**Pandas**, **NumPy**, **Scikit-learn**) to model prosthetic degradation, improving material-effectiveness prediction accuracy by **25%**

Projects

ReVal, West Lafayette, IN — *Software Project Manager* **Jan 2026 – May 2026**
- Led a **cross-functional team of 7** to build a full-stack **React**/**Node.js** platform (**Firebase**, **Supabase**) generating recruiter talking points from unstructured resumes, cutting prep latency to **under 120 seconds**
- Improved matching precision by **35%** with a modular retrieval-based **LLM** system using semantic embeddings to align student experiences with company business pillars and core values

FPGA Raytracer **Jun 2026 – Aug 2026**
- **Real-time 3D raytracer** in **SystemVerilog** on a **Xilinx Artix-7**, streaming pixels to a **640x480 @ 60Hz** VGA display
- Built a **32-bit Q16.16 fixed-point** vector library mapped onto native **DSP48 slices**, and removed **all division and square-root operations** via pre-computed inverses and a **ray-sphere intersection** accepting un-normalized rays
- Sustained **18.4M rays/sec** at **100 MHz** — one intersection every **4 clock cycles** across ray generation, intersection, and **Lambertian shading** — with **SystemVerilog testbenches** catching fixed-point **overflow** pre-synthesis in **Vivado**

Technical Skills

Languages: Python, C, C++, C#, Java, JavaScript, TypeScript, SystemVerilog, PHP, MATLAB
AI/ML: LLM Fine-Tuning, RAG, Multi-Agent Systems, Reinforcement Learning (PPO), Computer Vision, Vector DBs, Embeddings, PyTorch, Scikit-learn, NumPy, Pandas
Hardware & Tools: SystemVerilog, Vivado, FPGA (Artix-7), Altium, KiCad, Isaac Sim, Jetson Nano, I2C, React, Node.js, Docker, Git, Linux, REST APIs, MySQL, ROS2

Awards

- Publication in Journal of Purdue Undergraduate Research (JPUR) **Jan 2026**
- 2x High Distinction Award *(1 of 10 out of 1045)*, Purdue Undergraduate Research Conference **Nov 2025 / Apr 2026**